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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/954,866	09/18/2001	Maya B. Gokhale	S-96,589	8486

35068 7590 12/22/2004

UNIVERSITY OF CALIFORNIA
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EXAMINER

BLAIR, DOUGLAS B

ART UNIT

PAPER NUMBER

2142

DATE MAILED: 12/22/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/954,866

Applicant(s)

GOKHALE, MAYA B.

Examiner

Douglas B Blair

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 18 September 2001.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-10 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-10 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claim 1-2 and 7 are rejected under 35 U.S.C. 102(e) as being anticipated by U.S. Patent Number 6,411,616 to Donahue et al..

3. As to claim 1, Donahue teaches a hybrid hardware/software packet filter comprising: rule compiling means for assembling packet acceptance rules and creating a rule table, and outputting said rule table (col. 27, line 55-col. 28, line 32); a configurable hardware circuit receiving said rule table and creating hardware circuits representing said rule table for applying said rule table to said packet and outputting a match bit vector indicating whether said packet matched a corresponding entry in said rule table (col. 27, line 55-col. 28, line 32); linking means for receiving said match bit vector for linking said match bit vector with said corresponding entry in said rule table and for directing said packet to a destination determined by said rule table (col. 27, line 55-col. 28, line 32).

4. As to claim 2, Donahue teaches the hybrid software/hardware packet filter as described in claim 1, wherein said configurable hardware circuit is mapped onto an FPGA (col. 27, line 55-col. 28, line 32).

5. As to claim 7, Donahue teaches a method of filtering incoming packets comprising the steps of: compiling a set of rules to be applied to incoming packets (col. 27, line 55-col. 28, line

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32); configuring hardware to crate circuits representative of said set of rules (col. 27, line 55-col. 28, line 32); comparing said incoming packets with said circuits representative of said set of rules (col. 27, line 55-col. 28, line 32); outputting a single bit indicative of whether a packet is accepted or rejected; linking said single bit with a rule table (col. 27, line 55-col. 28, line 32); and directing said incoming packets to destinations determined by said rule table (col. 27, line 55-col. 28, line 32).

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

7. Claims 3-6 and 8-10 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent Number 6,411,616 to Donahue et al. in view of U.S. Patent Application Publication Number 2004/0088567 by Lomotte.

8. As to claim 3, Donahue teaches claim 1; however Donahue does not explicitly teach an HDL entity definition.

Lamotte teaches a rule compiler means outputting an HDL description for an FPGA (paragraph 38).

It would have been obvious to one of ordinary skill in the Computer Networking art at the time of the invention to combine the teachings of Donahue regarding the implementation of a

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packet filter on programmable hardware with the teachings of Lamotte regarding the use of HDL because HDL is a common method for programming an FPGA (paragraph 38).

9. As to claim 4, Lamotte teaches the HDL description entity definition comprising a Very High Speed IC HDL description (paragraph 38).

10. As to claim 5, Lamotte teaches the HDL description entity definition comprising verilog (paragraph 38).

11. As to claims 6, 9, and 10, Donahue teaches the subject matter of claims 1 and 7, however Donahue does not explicitly teach logging and alert generating in case of suspicious packets.

Lamotte teaches logging and alert generating in case of suspicious packets (paragraph 37).

It would have been obvious to one of ordinary skill in the Computer Networking art at the time of the invention to combine the teachings of Donahue regarding the implementation of a packet filter on programmable hardware with the teachings of Lamotte regarding logging and alert generating in case of suspicious packets because such actions enhance security (paragraph 37).

12. As to claim 8, Donahue teaches the method of claim 7; however Donahue does not teach the use VHDL.

Lamotte teaches configuring hardware using VDHL entity definitions (paragraph 38).

It would have been obvious to one of ordinary skill in the Computer Networking art at the time of the invention to combine the teachings of Donahue regarding the implementation of a packet filter on programmable hardware with the teachings of Lamotte regarding configuring

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hardware using VDHL entity definitions because VHDL is a common method for programming an FPGA (paragraph 38).

Conclusion

13. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Douglas B Blair whose telephone number is 571-272-3893. The examiner can normally be reached on 8:30am-5pm Mon-Fri.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jack Harvey can be reached on 571-272-3896. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Douglas Blair

DBB

J. Blair Carsons
Primary Ex.
AU: 2145